CLAIMS

What is claimed is:

1. A fractional-N synthesizer comprises:

forward path operably coupled to produce an output frequency from a reference frequency and a feedback reference frequency that is based on a divider value;

configurable feedback path operably coupled to produce the feedback frequency, wherein the configurable feedback path includes:

first feedback path used to provide the feedback frequency when a fractional value of the divider value is within a range of fractional values; and

second feedback path used provide the feedback frequency when the fractional value of the divider value is not within the range of fractional values.

2. The fractional-N synthesizer of claim 1, wherein the forward path further comprises:

phase-frequency detector operably coupled to receive the reference frequency and the feedback frequency, wherein the phase-frequency detector produces a difference signal based on the phase-frequency difference between the reference frequency and the feedback frequency;

charge pump operably coupled to receive the difference signal and produce therefrom a charge-up signal or a charge-down signal;

low pass filter operably coupled to filter the charge-up signal or the charge-down signal to produce a filtered signal; and

controlled oscillator operably coupled to produce the output frequency based on the filtered signal.

3. The fractional-N synthesizer of claim 1, wherein the configurable feedback path further comprises:

sigma delta modulator operably couple to receive the fractional value or a modified fractional value and produce therefrom a reference digital signal;

summing module operably coupled to sum the reference digital signal with an integer value of the divider value or a modified integer value to produce a first divider select signal;

multiplexor operably coupled to provide an output of the first feedback path as a partial feedback frequency when the fractional value of the divider value is within the range of fractional values and to provide an output of the second feedback path as the partial feedback frequency when the fractional value of the divider value is not within the range of fractional values; and

selectable divider operably coupled to produce the feedback frequency from the partial feedback frequency based on the first divider select signal.

4. The fractional-N synthesizer of claim 3, wherein the first feedback path further comprises:

a fixed divider that divides the output frequency by a fixed integer value to produce the partial feedback frequency.

5. The fractional-N synthesizer of claim 4, wherein the fixed divider divides the output frequency by a fixed integer value to produce an I component and a Q component of the output frequency, wherein the second feedback path further comprises;

second selectable divider that divides the I and Q components of the output frequency by a selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

6. The fractional-N synthesizer of claim 3, wherein the second feedback path further comprises:

quadrature module operably coupled to produce an I component and a Q component of the output frequency;

second selectable divider that divides the I and Q components of the output frequency by selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

7. The fractional-N synthesizer of claim 3, second feedback path further comprises:

quadrature module operably coupled to produce an I component and a Q component of the output frequency;

second selectable divider that divides I and Q components of the reference frequency by selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

8. The fractional-N synthesizer of claim 3 further comprises:

controller operably coupled to the configurable feedback path, wherein the controller determines when the fractional value of the divider value is within the range of fractional values, wherein the controller determines the modified fractional value and the modified integer value when the fractional value of the divider value is not within the range of fractional values, and wherein the controller generates a control signal that causes the multiplexor to provide the output of the first feedback path or the output of the second feedback path as the partial feedback frequency.

9. A method for fractional-N synthesis, the method comprises:

generating a first feedback frequency from an output frequency based on a fixed divider value, a fractional value of a divider value, and an integer value of a divider value, wherein the divider value and the fixed divider value indicate a ratio between a reference frequency and the output frequency;

generating a second feedback frequency from the output frequency based on a selectable divider value, a modified fractional value of the divider value, and a modified integer value of the divider value;

utilizing the first feedback frequency to produce the output frequency when the fractional value is within a range of fractional values; and

utilizing the second feedback frequency to produce the output frequency when the fractional value is not within the range of fractional values.

10. The method of claim 9, wherein the generating the first feedback frequency further comprises:

generating a first partial feedback frequency by dividing the output frequency by a fixed divider value;

sigma delta modulating the fractional value to produce a digital reference signal;

summing the digital reference signal with the integer value to produce a divider signal;

dividing the first partial feedback frequency in accordance with the divider signal to produce the first feedback frequency.

11. The method of claim 9, wherein the generating the second feedback frequency further comprises:

dividing the output frequency by a fixed integer value to produce an I component and a Q component of the output frequency;

dividing the I and Q components of the output frequency by the selectable divider value to produce a reference I frequency and a reference Q frequency;

mixing the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

mixing the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback frequency.

12. The method of claim 11 further comprises:

sigma delta modulating the modified fractional value to produce a digital reference signal; and

summing the digital reference signal with the modified integer value to produce the divider signal.

13. The method of claim 12 further comprises:

determining the modified fractional value based on the selected divider value; and

determining the modified integer value based on the selected divider value.

14. The method of claim 9, wherein the generating the second feedback frequency further comprises:

dividing the reference frequency by a fixed integer value to produce an I component and a Q component of the reference frequency;

dividing the output frequency by a second fixed integer value to produce an I component and a Q component of the output frequency;

mixing the I component of the output frequency with the I component of the reference frequency to produce a first mixed frequency;

mixing the Q component of the output frequency with the Q component of the reference frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback signal.

15. A method for fractional-N synthesis, the method comprises:

determining a fractional value of divider value, wherein the divider value represents at least a portion of a ratio between a reference frequency and an output frequency;

when the fractional value is outside a range of fractional values, selecting a partial divider value;

determining a modified fractional value and a modified integer value of the divider value based on the partial divider value;

generating a feedback frequency based on the partial divider value, the modified fractional value, and the modified integer value; and

generating the output frequency from the reference frequency and the feedback frequency.

16. The method of claim 15 further comprises:

when the fractional value is within the range of fractional values, generating the feedback frequency based on a fixed divider value, the fractional value, and an integer value of the divider value.

17. The method of claim 16, wherein the generating the feedback frequency further comprises:

generating a first partial feedback frequency by dividing the output frequency by the fixed divider value;

sigma delta modulating the fractional value to produce a digital reference signal;

summing the digital reference signal with the integer value to produce a divider signal; and

dividing the first partial feedback frequency in accordance with the divider signal to produce the feedback frequency.

18. The method of claim 15, wherein the generating the feedback frequency further comprises:

dividing the output frequency by a fixed integer value to produce an I component and a Q component of the output frequency;

dividing the I and Q components of the output frequency by the partial divider value to produce a reference I frequency and a reference Q frequency;

mixing the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

mixing the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the feedback frequency.

19. The method of claim 18 further comprises:

sigma delta modulating the modified fractional value to produce a digital reference signal; and

summing the digital reference signal with the modified integer value to produce the divider signal.

20. The method of claim 15, wherein the generating the feedback frequency further comprises:

dividing the reference frequency by a fixed integer value to produce an I component and a Q component of the reference frequency;

dividing the output frequency by a second fixed integer value to produce an I component and a Q component of the output frequency;

mixing the I component of the output frequency with the I component of the reference frequency to produce a first mixed frequency;

mixing the Q component of the output frequency with the Q component of the reference frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback signal.

21. A fractional-N synthesizer comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

generate a first feedback frequency from an output frequency based on a fixed divider value, a fractional value of a divider value, and an integer value of the divider value, wherein the divider value and the fixed divider value indicate a ratio between a reference frequency and the output frequency;

generate a second feedback frequency from the output frequency based on a selectable divider value, a modified fractional value of the divider value, and a modified integer value of the divider value;

utilize the first feedback frequency to produce the output frequency when the fractional value is within a range of fractional values; and

utilize the second feedback frequency to produce the output frequency when the fractional value is not within the range of fractional values.

22. The fractional-N synthesizer of claim 21, wherein the memory further comprises operational instructions that cause the processing module to generate the first feedback frequency by:

generating a first partial feedback frequency by dividing the output frequency by a fixed divider value;

sigma delta modulating the fractional value to produce a digital reference signal;

summing the digital reference signal with the integer value to produce a divider signal;

dividing the first partial feedback frequency in accordance with the divider signal to produce the first feedback frequency.

23. The fractional-N synthesizer of claim 21, wherein the memory further comprises operational instructions that cause the processing module to generate the second feedback frequency by:

dividing the output frequency by a fixed integer value to produce an I component and a Q component of the output frequency;

dividing the I and Q components of the output frequency by the selectable divider value to produce a reference I frequency and a reference Q frequency;

mixing the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

mixing the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback frequency.

24. The fractional-N synthesizer of claim 23, wherein the memory further comprises operational instructions that cause the processing module to:

sigma delta modulate the modified fractional value to produce a digital reference signal; and

sum the digital reference signal with the modified integer value to produce the divider signal.

25. The fractional-N synthesizer of claim 24, wherein the memory further comprises operational instructions that cause the processing module to:

determine the modified fractional value based on the selected divider value; and

determine the modified integer value based on the selected divider value.

26. The fractional-N synthesizer of claim 21, wherein the memory further comprises operational instructions that cause the processing module to generate the second feedback frequency by:

dividing the reference frequency by a fixed integer value to produce an I component and a Q component of the reference frequency;

dividing the output frequency by a second fixed integer value to produce an I component and a Q component of the output frequency;

mixing the I component of the output frequency with the I component of the reference frequency to produce a first mixed frequency;

mixing the Q component of the output frequency with the Q component of the reference frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback signal.

27. A fractional-N synthesizer comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

determine a fractional value of divider value, wherein the divider value represents at least a portion of a ratio between a reference frequency and an output frequency;

when the fractional value is outside a range of fractional values, select a partial divider value;

determine a modified fractional value and a modified integer value of the divider value based on the partial divider value;

generate a feedback frequency based on the partial divider value, the modified fractional value, and the modified integer value; and

generate the output frequency from the reference frequency and the feedback frequency.

28. The fractional-N synthesizer of claim 27, wherein the memory further comprises operational instructions that cause the processing module to:

when the fractional value is within the range of fractional values, generate the feedback frequency based on a fixed

divider value, the fractional value, and an integer value of the divider value.

29. The fractional-N synthesizer of claim 28, wherein the memory further comprises operational instructions that cause the processing module to generate the feedback frequency by:

generating a first partial feedback frequency by dividing the output frequency by the fixed divider value;

sigma delta modulating the fractional value to produce a digital reference signal;

summing the digital reference signal with the integer value to produce a divider signal; and

dividing the first partial feedback frequency in accordance with the divider signal to produce the feedback frequency.

30. The fractional-N synthesizer of claim 27, wherein the memory further comprises operational instructions that cause the processing module to generate the feedback frequency by:

dividing the output frequency by a fixed integer value to produce an I component and a Q component of the output frequency;

dividing the I and Q components of the output frequency by the partial divider value to produce a reference I frequency and a reference Q frequency;

mixing the reference I frequency with the I component of the output frequency to produce a first mixed frequency;

mixing the reference Q frequency with the Q component of the output frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the feedback frequency.

31. The fractional-N synthesizer of claim 30, wherein the memory further comprises operational instructions that cause the processing module to:

sigma delta modulate the modified fractional value to produce a digital reference signal; and

sum the digital reference signal with the modified integer value to produce the divider signal.

32. The fractional-N synthesizer of claim 27, wherein the memory further comprises operational instructions that cause the processing module to generate the feedback frequency by:

dividing the reference frequency by a fixed integer value to produce an I component and a Q component of the reference frequency;

dividing the output frequency by a second fixed integer value to produce an I component and a Q component of the output frequency;

mixing the I component of the output frequency with the I component of the reference frequency to produce a first mixed frequency;

mixing the Q component of the output frequency with the Q component of the reference frequency to produce a second mixed frequency;

summing the first and second mixed frequencies to produce a partial feedback frequency; and

dividing the partial feedback frequency based on a divider signal to produce the second feedback signal.

33. An integrated radio comprises:

radio frequency receiver section operably coupled to receive an inbound radio frequency signal and a clock signal, wherein the radio frequency receiver section converts the inbound radio frequency signal into an inbound intermediate frequency signal;

radio frequency transmitter section operably coupled to receive an outbound intermediate frequency signal and the clock signal, wherein the radio frequency transmitter section converts the outbound intermediate frequency signal into an outbound radio frequency signal;

oscillation module operably coupled to produce a reference frequency;

local oscillator that includes:

summing module;

divider module;

a fractional-N synthesizer that includes:

forward path operably coupled to produce an output frequency from the reference frequency and a feedback reference frequency that is based on a divider value;

configurable feedback path operably coupled to produce the feedback frequency, wherein the configurable feedback path includes:

first feedback path used to provide the feedback frequency when a fractional value of the divider value is within a range of fractional values; and

second feedback path used provide the feedback frequency when the fractional value of the divider value is not within the range of fractional values, wherein the divider module divides the output frequency to produce a divided frequency and wherein the summing module sums the output frequency and the divided frequency to produce the clock signal.

34. The integrated radio of claim 33 further comprises:

the radio frequency receiver section operable to convert the inbound radio frequency signal into one of a plurality of inbound intermediate frequency signals, wherein the plurality of inbound intermediate frequency signals includes the inbound intermediate frequency signal; and

the radio frequency transmitter section operable to convert one of a plurality of outbound intermediate frequency signals into the outbound radio frequency signal, wherein the plurality of outbound intermediate frequency signals includes the outbound intermediate frequency signal.

35. The integrated radio of claim 33, wherein the forward path further comprises:

phase-frequency detector operably coupled to receive the reference frequency and the feedback frequency, wherein the phase-frequency detector produces a difference signal based on the phase-frequency difference between the reference frequency and the feedback frequency;

charge pump operably coupled to receive the difference signal and produce therefrom a charge-up signal or a charge-down signal;

low pass filter operably coupled to filter the charge-up signal or the charge-down signal to produce a filtered signal; and

controlled oscillator operably coupled to produce the clock signal based on the filtered signal.

36. The integrated radio of claim 33, wherein the configurable feedback path further comprises:

sigma delta modulator operably couple to receive the fractional value or a modified fractional value and produce therefrom a reference digital signal;

summing module operably coupled to sum the reference digital signal with an integer value of the divider value

or a modified integer value to produce a first divider select signal;

multiplexor operably coupled to provide an output of the first feedback path as a partial feedback frequency when the fractional value of the divider value is within the range of fractional values and to provide an output of the second feedback path as the partial feedback frequency when the fractional value of the divider value is not within the range of fractional values; and

selectable divider operably coupled to produce the feedback frequency from the partial feedback frequency based on the first divider select signal.

37. The integrated radio of claim 36, wherein the first feedback path further comprises:

a fixed divider that divides the clock signal by a fixed integer value to produce the partial feedback frequency.

38. The integrated radio of claim 37, wherein the fixed divider divides the clock signal by a fixed integer value to produce an I component and a Q component of the output frequency, wherein the second feedback path further comprises;

second selectable divider that divides the I and Q components of the clock signal by a selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the clock signal to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the clock signal to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

39. The integrated radio of claim 36, wherein the second feedback path further comprises:

quadrature module operably coupled to produce an I component and a Q component of the clock signal;

second selectable divider that divides the I and Q components of the clock signal by selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the clock signal to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the clock signal to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

40. The integrated radio of claim 36, second feedback path further comprises:

quadrature module operably coupled to produce an I component and a Q component of the reference frequency;

second selectable divider that divides the I and Q components of the reference frequency by selected divisor to produce a reference I frequency and a reference Q frequency;

I mixer operably coupled to mix the reference I frequency with the I component of the clock signal to produce a first mixed frequency;

Q mixer operably coupled to mix the reference Q frequency with the Q component of the clock signal to produce a second mixed frequency; and

summing module that sum the first and second mixed frequencies to produce the partial feedback frequency.

41. The integrated radio of claim 36 further comprises:

controller operably coupled to the configurable feedback path, wherein the controller determines when the fractional value of the divider value is within the range of fractional values, wherein the controller determines the modified fractional value and the modified integer value when the fractional value of the divider value is not within the range of fractional values, and wherein the

controller generates a control signal that causes the multiplexor to provide the output of the first feedback path or the output of the second feedback path as the partial feedback frequency.